PATENT ABSTRACTS OF JAPAN

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(54) RATE CONVERSION METHOD AND ITS CONVERSION CIRCUIT

(57)Abstract:
PURPOSE: To provide a rate conversion method and its conversion circuit able to obtain a sufficient characteristic practically from a ROM of even a small capacity.
CONSTITUTION: The conversion circuit is provided with a digital filter 13 receiving a 1st digital signal D11 to implement oversampling for a multiple of (m) (m>2 being an integral number) of a 1st sampling frequency and with an interpolation circuit 15 implementing linear interpolation with respect to an input signal. Operation by the digital filter 13 is applied to the 1st digital signal D11 at points of 1st and 2nd times having a 2nd digital signal D15 before and after inbetween timewise among point of times t1-tm being m-equal divisions of a period of the 1st digital signal D15. The result of the operation at the 1st and 2nd point of times is fed to the interpolation circuit 15, from which a 2nd digital signal D15 is obtained.

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CLAIMS

[Claim(s)]

[Claim 1] [when carrying out rate conversion of the 1st digital signal of the 1st sampling frequency at the 2nd digital signal of the 2nd sampling frequency] It asks for the time of doing m division into equal parts (integer of m> 2) of the period of the 1st digital signal of the above. The inside at the time of [this] doing m division into equal parts of, When [1st and 2nd] inserting the 2nd digital signal of the above from order in time The rate conversion approach of performing m times [above-mentioned] as many over sampling technique as this to the 1st digital signal of the above, carrying out linear interpolation of the result of the above-mentioned over sampling technique at the 1st and 2nd times of the above, and having acquired the 2nd digital signal of the above.

[Claim 2] [when carrying out rate conversion of the 1st digital signal of the 1st sampling frequency at the 2nd digital signal of the 2nd sampling frequency] When making periodicity of the 2nd digital signal of the above in the period of the least common multiple of the 1st digital signal of the above, and the 2nd digital signal of the above into m-n (m and n are two or more integers), It asks for the time of doing m division into equal parts of the period of the 1st digital signal of the above. The inside at the time of [this] doing m division into equal parts of, When [2nd] continuing at these 1st and 1st times in front of the 2nd digital signal of the above, m times as many over sampling technique as this is performed to the 1st digital signal of the above. The 1st time of the above, It asks for the time of doing n division into equal parts of the period during the 2nd time of the above. The inside at the time of [this] doing n division into equal parts of, The rate conversion approach which carries out linear interpolation of the result of the above-mentioned [the data at the time of a time amount location being in agreement] over sampling technique at the 1st and 2nd times of the above, asks the 2nd digital signal of the above for it, and took out the data based on this linear interpolation as the 2nd digital signal of the above.

[Claim 3] In the rate conversion circuit which carries out rate conversion of the 1st digital signal of the 1st sampling frequency at the 2nd digital signal of the 2nd sampling frequency The digital filter which the 1st digital signal of the above is

supplied and performs m times (integer of m> 2) as much over sampling technique as the 1st sampling frequency of the above, It has the interpolation circuit which performs linear interpolation to an input signal. The period of the 1st digital signal of the above m division into equal parts The inside at the time of carrying out, When [1st and 2nd] inserting the 2nd digital signal of the above from order in time The rate conversion circuit which calculates the above-mentioned digital filter to the 1st digital signal of the above, supplies the result of the above-mentioned operation at the 1st and 2nd times of the above to the above-mentioned interpolation circuit, and acquired the 2nd digital signal of the above.

[Claim 4] In the rate conversion circuit which carries out rate conversion of the 1st digital signal of the 1st sampling frequency at the 2nd digital signal of the 2nd sampling frequency When making periodicity of the 2nd digital signal of the above in the period of the least common multiple of the 1st digital signal of the above, and the 2nd digital signal of the above into m-n (m and n are two or more integers), The 1st digital signal of the above is supplied, have the digital filter which performs m times as much over sampling technique as the 1st sampling frequency of the above, and the interpolation circuit which performs linear interpolation to an input signal, and it sets to the above-mentioned digital filter. The period of the 1st digital signal of the above m division into equal parts when [1st and 2nd] inserting the 2nd digital signal of the above from order in time in at the time of carrying out Perform m times as many over sampling technique as this to the 1st digital signal of the above, and it sets to the above-mentioned interpolation circuit. The period during the 1st and 2nd time of the above of the above n division into equal parts The inside at the time of carrying out, The rate conversion circuit which carries out linear interpolation of the result of the above-mentioned [the data at the time of a time amount location being in agreement] over sampling technique at the 1st and 2nd times of the above, asks the 2nd digital signal of the above for it, and took out the data based on this linear interpolation as the 2nd digital signal of the above.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the rate conversion approach of digital data, and its conversion circuit.

[0002]

[Description of the Prior Art] For example, generally in the digital audio device, 48kHz, 44.1kHz, and 32kHz are used as a sampling frequency of a digital audio signal.

[0003] For this reason, modification of that sampling frequency, i.e., rate conversion, may be needed to a digital audio signal.
[0004] and approach ** changed by ** linear interpolation as the approach of this rate conversion -- how to carry out direct conversion by alternative over sampling technique is considered.
[0005] That is, in the case of the approach of **, the analog audio signal of a basis is shown by the curve of the continuous line of drawing 5 B, and if the clock before rate conversion (A/D-conversion point) is shown by drawing 5 A, the digital audio signal before rate conversion serves as data which put - mark in drawing 5 B. And if the clock after rate conversion is shown by drawing 5 C, as a broken line shows, it assumes the straight line which connects these - mark, and takes out the data which put the x mark as a digital audio signal which carried out rate conversion.
[0006] Moreover, in the case of the approach of **, let the least common multiple of the sampling frequency of the digital audio signal before rate conversion, and the sampling frequency of the digital audio signal after rate conversion be the frequency of over sampling technique. And actual count is performed about the over sampling technique point before the rate conversion which is in agreement with the sampling point after conversion, and the digital audio signal by which rate conversion was carried out is obtained.
[0007]
[Problem(s) to be Solved by the Invention] However, in the case of the approach of **, for linear interpolation, the error of the level in the digital audio signal after rate conversion may become large so that clearly also from drawing 5 . Furthermore, a clinch component cannot fully be attenuated.
[0008] Moreover, since the frequency of over sampling technique becomes with the least common multiple of the sampling frequency of the digital audio signal before rate conversion, and the sampling frequency of the digital audio signal after rate conversion in the case of the approach of **, when the combination of the rate to change is 44.1kHz and 48kHz, the least common multiple will become large and the multiple or frequency of over sampling technique will become very high. Consequently, the number of the multiplication circuits of the digital filter used for over sampling technique will increase extremely, and the thing of a capacity huge as a ROM which gives that multiplication multiplier will be needed.
[0009] This invention tends to solve the above troubles.
[0010]
[Means for Solving the Problem] For this reason, in this invention, if the reference mark of each part is made to correspond to the below-mentioned example [when carrying out rate conversion of the 1st digital signal D11 of the 1st sampling frequency at the 2nd digital signal D15 of the 2nd sampling frequency] The digital filter 13 which the 1st digital signal D11 is supplied and performs m times as much over sampling technique as the 1st sampling frequency, It is t1 -tm the time of

forming the interpolation circuit 15 which performs linear interpolation to an input signal, and doing m division into equal parts of the period tau of the 1st digital signal D11. Inside, When [1st and 2nd] inserting the 2nd digital signal D15 from order in time A digital filter 13 is calculated to the 1st digital signal D11, the result of the operation at the 1st and 2nd times is supplied to an interpolation circuit 15, and the 2nd digital signal D15 is acquired.

[0011]

[Function] While over sampling technique of the 1st digital signal D11 is carried out in a digital filter 13 by the multiple m from which a required property is acquired, the over sampling technique is performed at the two times which sandwiches the 2nd digital signal D15 from order in time. And linear interpolation of the result of this over sampling technique is carried out by the interpolation circuit 15, and the 2nd digital signal D15 is taken out.

[0012]

[Example] In drawing 1 , the clock P21 which synchronized with the digital audio signal before rate conversion is supplied to the signal formation circuit 22 through a terminal 21, various kinds of control signals and timing signals are formed, and these signals are supplied to the below-mentioned circuits 12-16, respectively. Moreover, in the formation circuit 22, the clock P27 which synchronized with the digital audio signal after rate conversion is also formed, and this clock P27 is taken out by the terminal 27.

[0013] Drawing 3 A shows a clock P21, drawing 3 C shows a clock P27, clocks P21 and P27 are the periods of the least common multiple, and its time amount location corresponds. in addition, the time of a clock P21 being located -- Time T -- the period is set to tau while considering as 1, T2, T3, and .....

[0014] And the digital audio signal D11 before rate conversion is supplied to a digital filter 13 through the input interface circuitry 12 from a terminal 11. In this example, a filter 13 performs 4 times as many over sampling technique as this to a signal D11. For this reason, a filter 13 is five steps of delay circuits DL11-DL15 where a signal D11 is supplied to a serial as shown in drawing 2 , and a signal D11 and delay circuits DL11-DL15. It is constituted by the FIR mold by the multiplication circuits MP11-MP16 which are six to which a delay output is supplied, and the adder circuit SM 11 to which that multiplication output is supplied.

[0015] Furthermore, 14 is ROM for multipliers, and a predetermined thing is chosen among those multiplication multiplier k1 -K25, and it is set to the multiplication circuits MP11-MP16 while the multiplication multiplier used for this ROM14 in the multiplication circuits MP11-MP16, multiplication multiplier k1 -k25 [for example,] as shown in drawing 3 E, is written in.

[0016] And that over sampling technique point is t1 -t4 the time of dividing the period tau of a clock P21 into four equally, as it is shown in drawing 3 B, since a filter 13 performs 4 times as many over sampling technique as this in this example. It becomes.

[0017] and -- if it is original -- this -- all -- all the times of a period tau -- t1 -t4 While needing the operation of a filter 13, it is necessary to set each multiplication multiplier to the multiplication circuits MP11-MP16 from ROM14 for every operation of that.

[0018] however, this invention is shown in drawing 3 B-D -- as -- for example, a time -- T four a time -- T5 if it is the period of a between -- a clock P27 -- a time -- t3 a time -- t4 since it is located at the period of a between -- this time -- t3 a time -- t4 ******** -- the operation of a filter 13 is performed. namely, -- general -- a time -- t1 - the operation of a filter 13 is performed only in t4 the time in front of inside and a clock P27 -- a time -- tj then, this time -- tj Time t of continuing (j+1) (j is either 1-4.) It is referred to as j+1=1 at the time of j= 4.

[0019] for example, a time -- T four a time -- T5 the time of the period of a between -- t3 it is -- if -- The inside of multiplication multiplier k1 -K25 (drawing 3 E) currently written in ROM14, - As the multiplier k3 in every [which put the mark] four, k7, and k11, k15, k19 and k23 are taken out from ROM14 and this taken-out multiplication multiplier shows drawing 2 , it is set to the multiplication circuits MP11-MP16 of a filter 13, and an operation is performed.

[0020] And the operation output of this filter 13 is supplied to the linear interpolation circuit 15. this interpolation circuit 15 is shown in drawing 4 A-C -- as (drawing 4 has expanded the time-axis to drawing 3) -- a time -- tj and t (j+1) the operation output of the filter 13 which can be set -- values Dj and D (j+1) Then, these values Dj and D (j+1) from -- value [linear interpolation] Di at the time of a clock P27 It computes.

[0021] In this way, from an interpolation circuit 15, it is the data Di at the time of the clock P27 every clock P27. It is taken out.

[0022] This taken-out data Di Since it is obtained every clock P27 after rate conversion, it is exactly the digital audio signal by which rate conversion was carried out. Then, this data D15 (= Di) is outputted to a terminal 17 through the output interface circuitry 16 as a digital audio signal D15 by which rate conversion was carried out.

[0023] In this way, although rate conversion of a digital audio signal can be performed, generally it is as follows.

[0024] 1. Periodicity of a signal D15 in the period of the least common multiple of the signal D11 (clock P21) before rate conversion and the signal D15 (clock P27) after rate conversion is made into m-n (m and n are two or more integers).

2. The digital filter 13 which performs m times as much over sampling technique as the sampling frequency of the signal D11 before rate conversion is formed.

3. Form the interpolation circuit 15 which performs linear interpolation to the output of a filter 13.

4. It is t1 -tm the time of doing m division into equal parts of the period tau of the signal D11 before rate conversion. It sets.

5. a time -- t1 - perform the operation of a filter 13 only in tm the time in front of the clock P27 after [inner] rate conversion -- a time -- tj ** -- the time of carrying out -- this time -- tj Time t of continuing (j+1) (either j1-m) It is referred to as j+1=1 at the time of j=m. About this result of an operation, they are a value Dj and D (j+1). It carries out.
6. a time -- tj Time t (j+1) n division into equal parts of the period of a between is done.
7. one of the times at the time of being based on n division into equal parts -- ti since it is in agreement with 1. term at the time of the signal D15 after rate conversion -- this time of being in agreement -- ti Value Di which can be set A value Dj and D (j+1) from -- it asks by linear interpolation. namely, a Di =(D (j+1)-Dj) (N/n)+DjN:time -- tj from -- a time -- ti Sequence to value Di It asks.
8. This calculated value Di It outputs as a signal D15 by which rate conversion was carried out.
If it is made above, rate conversion of arbitration can be performed.
[0025] However, although the magnitude of attenuation of a clinch component can be enlarged if a value m is enlarged in that case, in proportion to this value m, the capacity of ROM14 will become large.
[0026] Then, a value m is chosen as the minimum value which can permit a clinch component in this invention. And if it is made such, capacity of ROM14 can be set to 1/n in the case of the approach of ** mentioned above.
[0027] That is, the value m small to extent from which the rate transfer characteristic serves as necessary minimum since it is meaningless even if there is a limitation in the property of the signal D11 before rate conversion etc. in fact although the rate transfer characteristic will become good so much theoretically if a value m is enlarged, and it improves only the rate transfer characteristic is chosen, and a value n is enlarged. If it is made such, capacity of ROM14 can be set to 1/n.
[0028] For example, it is m-n=320 if it is the case where rate conversion of the sampling frequency is carried out from 44.1kHz at 32kHz. Although it becomes, m= 40, i.e., the over sampling technique of a filter 13, is made into 40 times, for example. Then, it is set to n= 8 and the capacity of ROM14 can be reduced to one eighth.
[0029]
[Effect of the Invention] According to this invention, since the digital filter 13 and the linear interpolation circuit 15 were made to perform rate conversion, capacity of ROM14 for multipliers of a digital filter 13 can be made small to 1/n.
[0030] Moreover, since the number of multiplication multipliers required for 1 set of rate conversion is set to 1/n, all the multiplication multipliers required for two or more sets of rate conversion can also be prepared for ROM14, and the conversion circuit which can respond to two or more rate translation modes can be realized by LSI of one chip.
[0031] Furthermore, although the count of an operation and the operation time of

over sampling technique in a filter 13 pose a problem when the big value as a value m is required a time before and after inserting the signal D15 (clock P27) after rate conversion in this invention -- tj and t (j+1) ********, since what is necessary is just to calculate over sampling technique That is, since the signal D15 twice the number of after rate conversion should just calculate over sampling technique, while the count of an operation is not influenced by the value m, a leeway is given in the processing time.

[0032] Moreover, although ROM14 has all multiplication multiplier k1 -k25 [required for 4 times as many over sampling technique as this] By one operation, as shown in drawing 2 , the multiplication multiplier of the location of drawing 3 E, for example, - mark, i.e., the multiplication multiplier of every four of multiplication multiplier k1 -k25 (=m) Since it is only used, setting to the multiplication circuits MP11-MP16, the operation time needed for the count of an operation not changing with the magnitude of a value m, therefore asking for one sample of a signal D15 is not influenced by the value m, either.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the schematic diagram showing an example of this invention.

[Drawing 2] It is the schematic diagram showing some examples of drawing 1 .

[Drawing 3] It is drawing for explaining actuation of drawing 1 .

[Drawing 4] It is drawing for explaining actuation of drawing 1 .

[Drawing 5] It is drawing for explaining the conventional example.

[Description of Notations]

12 Input Interface Circuitry

13 Digital Filter

14 ROM for Multipliers

15 Linear Interpolation Circuit

16 Output Interface Circuitry

22 Signal Formation Circuit
